WHAT IS CLAIMED IS:

1. An output buffer circuit comprising:

a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node, and a first pull-down transistor controlled by a second input signal and a second pull-down transistor controlled by a third input signal are connected in series between said common node and a low-potential power supply;

an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits; and

first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point.

2. An output buffer circuit comprising:

a plurality of unit circuits in each of which a plurality of pull-up transistors controlled by an input signal are connected in series between a high-potential power supply and common node, and a plurality pull-down transistors controlled by an input signal are connected in series between said common node and a low-potential power supply;

an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits; and

first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point.

3. A circuit according to claim 1, further comprising second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply in each of said plurality of unit circuits.

4. A circuit according to claim 3, wherein said

plurality of second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply have the same resistance.

5. A circuit according to claim 2, further comprising third resistors formed respectively between said pull-up transistors and common node and between said common node and pull-down transistors in each of said plurality of unit circuits.

6. A circuit according to claim 5, wherein said plurality of third resistors formed respectively between said pull-up transistors and common node and between said common node and pull-down transistors have the same resistance.

7. A circuit according to claim 2, wherein said plurality of first resistors formed between said common nodes and output terminal have the same resistance.

8. A circuit according to claim 2, wherein each of said pull-up and pull-down transistors is a MIS transistor.

9. A circuit according to claim 2, wherein said plurality of pull-up transistors have the same gate length and the same gate width, and said plurality of pull-down transistors have the same gate length and the same gate width.

10. A circuit according to claim 2, wherein said resistor is selected from the group consisting of a metal film, composite metal film, metal cermet film, polysilicon film, diffusion layer, and transistor.

11. An output buffer circuit comprising:

a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node, and a pull-down transistor controlled by a second input signal is connected between said common node and a low-potential power supply;

an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits; and

second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply in each of said unit circuits.

12. A circuit according to claim 11, wherein said plurality of second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply have the same resistance.

13. An output buffer circuit comprising:

a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node, and a pull-down transistor controlled by a second input signal is connected between said common node and a low-potential power supply;

an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits; and

third resistors formed respectively between said pull-up transistor and common node and between said common node and pull-down transistor in each of said unit circuits.

14. A circuit according to claim 13, wherein said plurality of third resistors formed respectively between said pull-up transistor and common node and between said common node and pull-down transistor have the same resistance.

15. A semiconductor memory comprising:

a plurality of memory cells;

a plurality of terminals including an output terminal; and

an output buffer circuit positioned adjacent to

said memory cell, said output buffer circuit comprising a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node and a pull-down transistor controlled by a second input signal is connected between said common node and a low-potential power supply, and comprising first resistors connected respectively between said common nodes of said plurality of unit circuits and a common connecting point of said common nodes.

16. A memory according to claim 15, wherein said first resistors are formed between said output buffer circuit and output terminal.

17. A memory according to claim 16, wherein if the number of said first resistors is an even number, said first resistors are symmetrically arranged with respect to a central line of said output buffer circuit and output terminal, and have the same value, the same size, and the same shape.

18. A memory according to claim 15, wherein said first resistors are formed on at least not less than one of three sides of said output terminal, which do not oppose said output buffer circuit.

19. A memory according to claim 18, wherein if the number of first resistors is two, said first resistors are symmetrically arranged in portions of said output terminal, which do not oppose said output buffer circuit, and have the same value, the same size, and the same shape.